Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **1A**
2. **1B**
3. **1Y**
4. **2A**
5. **2B**
6. **2Y**
7. **GND**
8. **3Y**
9. **3A**
10. **3B**
11. **4Y**
12. **4A**
13. **4B**
14. **VCC**

**.059”**

**.059”**

**13 12 11 10**

**14**

**1**

**2**

**3 4 5 6**

**9**

**8**

**7**

**11600H**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: SiN2**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VCC**

**Mask Ref: 11600H**

**APPROVED BY: DK DIE SIZE .059” X .059” DATE: 7/15/22**

**MFG: TIH / HARRIS THICKNESS .020” P/N: 54HC00**

**DG 10.1.2**

#### Rev B, 7/1